## REMARKS

Claim 1-19 are pending in the application. Claim 1 has been withdrawn and claims 2 and 11 have been amended by way of the present amendment.

In the outstanding Office Action, claims 2-9 and 11-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over by U.S. Patent No. 6,215,135 (Schroder) in view of U.S. Patent No. 5,589,423 (White et al.); and claims 10 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder in view of White et al. and further in view of Applicant's Admitted Prior Art (AAPA).

### *Rejections under 35 U.S.C. Section 103*

Claims 2-9 and 11-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder in view of White et al. Claims 2 and 11 have been amended to further clarify the invention. In particular, claims 2 and 11 have been amended to recite:

> wherein said gate is positioned between a p-diffusion of said source and a p-diffusion of said drain,
> an n-diffusion is directly connected to said gate and said p-diffusion of said source and the n-diffusion is spaced apart from said p-diffusion of said source (emphasis added).

Support for the amendments is provided at least at page 11, lines 1-16; and shown at least in FIG. 7 of the specification. In particular, FIG. 7 of the specification *clearly shows* that the n-diffusion **745** is *directly connected* to the gate **742** and p-diffusion **743** of the source. In addition, FIG. 7 *clearly shows* that the n-diffusion **745** is *spaced apart* from the p-diffusion **743** of the source. Therefore, it is respectfully submitted that the amendments raise no question of new matter.

Schroder discloses an integrated circuit provided with electrostatic discharge (ESD) protection means.[1] In particular, Schroder discloses a Metal Oxide Semiconductor (MOS) transistor device **MP** with a p-type substrate **SUBSTR** and an n-type well **WLL**.[2] Further, Schroder discloses the MOS transistor device **MP** includes a gate **g2**, located between p+ areas **d4**, **d5** that jointly form the MOS transistor device **MP**; an n+ area **d6** that is located adjacent to p+ area **d5** and is connected to a second reference terminal **VDD**; and a bonding

[1] Schroder at ABSTRACT.

pad ***BP*** connected to the p+ area **d4**.[3] More specifically Schroder discloses a protection means where there will be no current flowing though the substrate **SUBSTR** since the n-type well **WLL** is connected via the n+ area **d6** to a reference terminal **VDD**.[4]

However, Schroder nowhere discloses, as amended claims 2 and 11 clearly recite:

> *an n-diffusion is directly connected* to said gate and said p-diffusion of said source and *the n-diffusion is spaced apart* from said p-diffusion of said source (emphasis added).

That is, FIG. 7 of the specification *clearly shows* that the n-diffusion **745** is *directly connected* to the gate **742** and p-diffusion **743** of the source (emphasis added). In addition, FIG. 7 *clearly shows* that the n-diffusion **745** is *spaced apart* from the p-diffusion **743** of the source (emphasis added). In contrast to the recitations of claims 2 and 11 and the illustration of FIG. 7 of the specification, Schroder clearly discloses, as shown in FIG. 1, an n+ area **d6** that is *located immediately adjacent* to p+ area **d5**. Thus, it is respectfully submitted that Schroder clearly does *not* disclose the limitations of the invention as recited in claims 2 and 11.

In addition, the outstanding Office Action acknowledges other deficiencies in Schroder and attempts to overcome these deficiencies with White et al.[5] However, White et al. cannot overcome the deficiencies of Schroder as discussed below.

White et al. discloses a process for fabricating a non-silicided region in an integrated circuit.[6] However, White et al. nowhere discloses, as claims 2 and 11 recite:

> *an n-diffusion* is *directly connected* to said gate and said p-diffusion of said source and *the n-diffusion is spaced apart* from said p-diffusion of said source (emphasis added).

That is, White et al. cannot overcome the deficiencies of Schroder, as discussed above.

Therefore, it is respectfully submitted that neither Schroder nor White et al. disclose, suggest or make obvious the claimed invention, whether taken individually or in combination, and therefore, claim 2 and claim 11, and claims dependent thereon, patentably distinguish thereover.

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[2] *Id.* at FIG. 1.
[3] *Id.* at column 2, lines 40-55.
[4] *Id.* at column 3, lines 5-10.
[5] Outstanding Office Action at page 3, lines 17-19.
[6] White et al. at ABSTRACT.

Claims 10 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder in view of White et al. and further in view of AAPA. Applicants respectfully traverse the rejection.

Claims 10 and 19 are ultimately dependent upon claims 2 and 11, respectively. Thus, at least for the reasons discussed above, neither Schroder nor White et al. disclose, suggest or make obvious the invention of claims 10 and 19.

In addition, the outstanding Office Action acknowledges deficiencies in Schroder and White et al. and attempts to overcome these deficiencies with AAPA.[7] However, AAPA cannot overcome the deficiencies of Schroder and White et al. as discussed below.

The AAPA discloses a circuit configuration of the background art typical of a latch-up condition.[8] However, it is respectfully submitted that the circuit configuration of the AAPA is not analogous to the recitations in claims 2, 10, 11 and 19. In particular, claims 2 and 11 recite:

> *an n-diffusion is directly connected to said gate and said p-diffusion of said source...* and
> said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain (emphasis added).

Moreover, claim 10 recites: a "p-type resistor is located between a p-diffusion of said drain of said transistor and said I/O pad" and claim 19 is similarly worded. That is, in the invention of claims 2 and 11, the I/O pad is connected to a *p-diffusion drain* of the transistor. Thus, in claims 10 and 19, the "p-type resistor" is located between the I/O pad and "a p-diffusion drain" of said transistor."

In contrast to the claimed invention, the AAPA discloses a resistor **R** located between an **INPUT PAD** and diodes **D1, D2**. That is, the AAPA nowhere discloses resistor R as connected to a "p-diffusion drain," as clearly recited in claims 10 and 19. Thus, it is respectfully submitted that, the AAPA does not disclose the limitations of claims 10 and 19 and cannot overcome the deficiencies of Schroder and White et al.

Therefore, it is respectfully submitted that none of Schroder, White et al. and AAPA, whether taken individually or in combination, disclose, suggest or make obvious the claimed

invention and that claims 10 and 19, and claims dependent thereon, patentably distinguish thereover.

***Conclusion***

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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[7] Outstanding Office Action at page 5, lines 15-17.
[8] Specification at page 3, lines 20-25.